Power Electronic Building Block Design and Hardware Demonstrator - Results From December 1996 Through May 1998

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Presented at the Power Systems World International Conference and Exhibit,

Santa Clara, CA November 11, 1998

Background

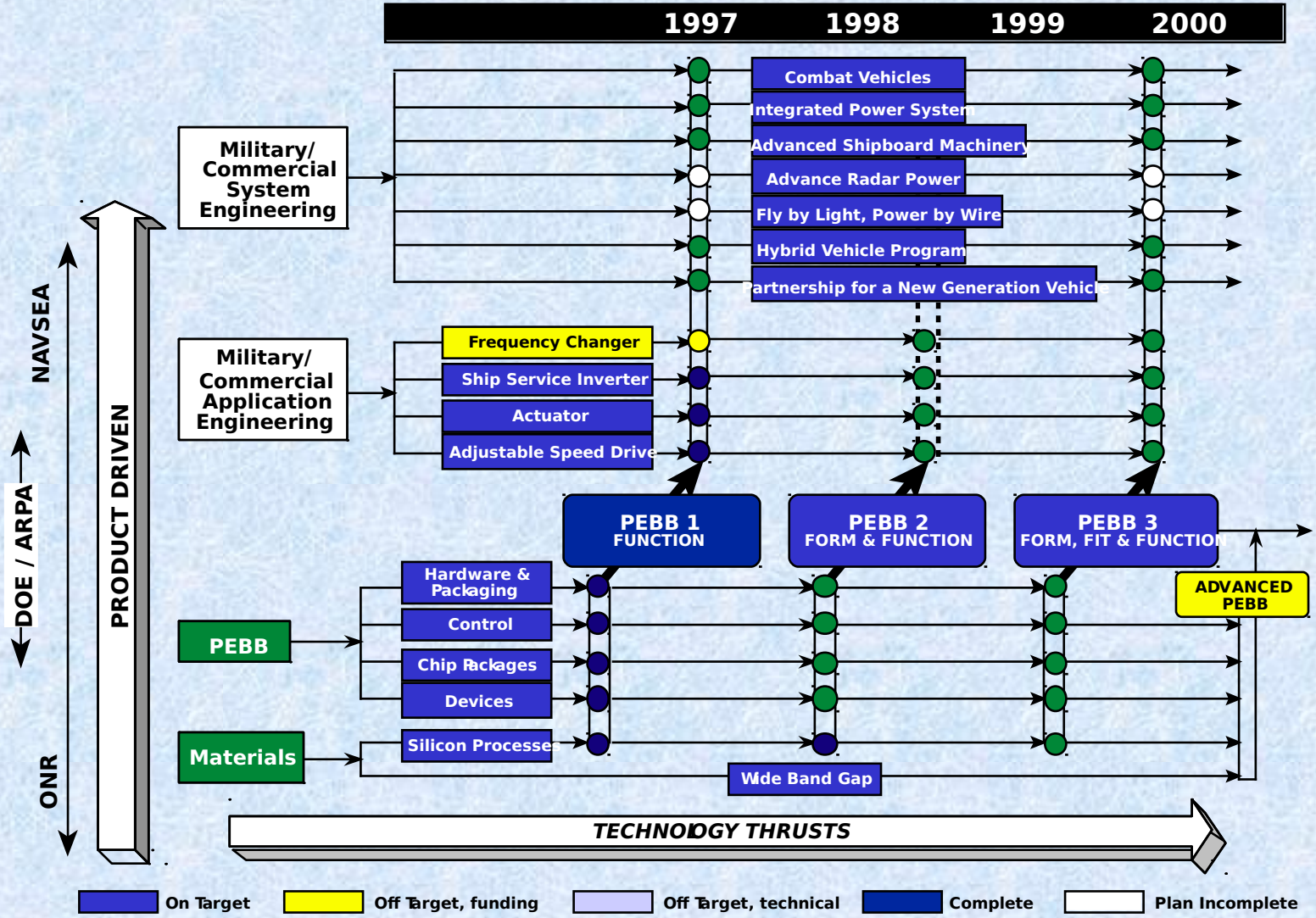
- The Naval Surface Warfare Center (NSWC), Carderock Division, Annapolis Detachment
  - Presently located in Annapolis, MD (soon to be Phila. PA)
  - Serves as one of the research and development arms of the US Navy
  - Area of expertise - Hull, Mechanical and Electrical (HM&E) aspects of US Navy ship design
  - Primarily funded by the Naval Sea Systems Command (NAVSEA) and the Office of Naval Research (ONR)

The Annapolis Detachment
of the Naval Surface Warfare Center, Carderock Division

Background

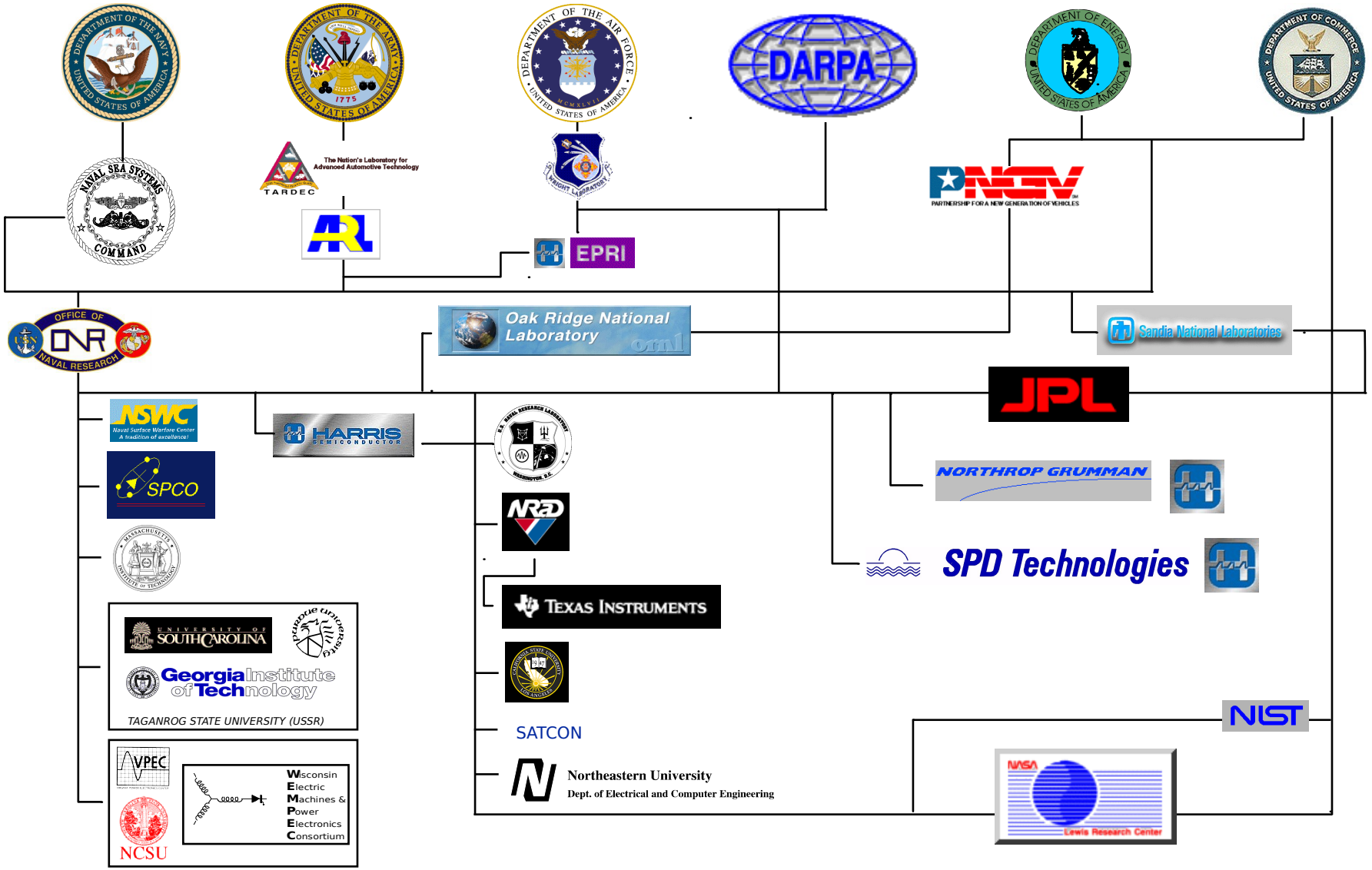
- This work was funded by the Office of Naval Research under the Power Electronic Building Block Program
- The goal of the PEBB program is to enable the application of more electric power conversion for US Navy ships through the affordable implementation of advanced electrical power conversion techniques and components.

PEBB Concurrent Development



Power Distribution Modules

PEBB Organization



Background

- NSWC was tasked to investigate the use of soft switching inverter technology in a multifunctional electrical power converter.
- Concurrently, ONR tasked Harris Semiconductor to team with NSWC to pro
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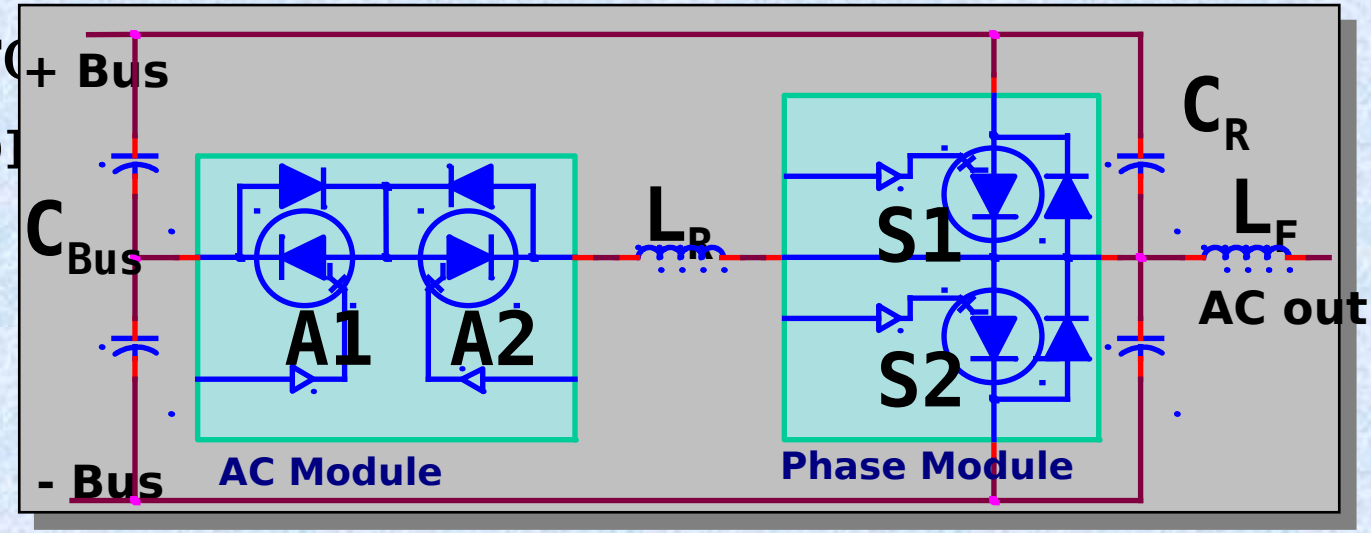
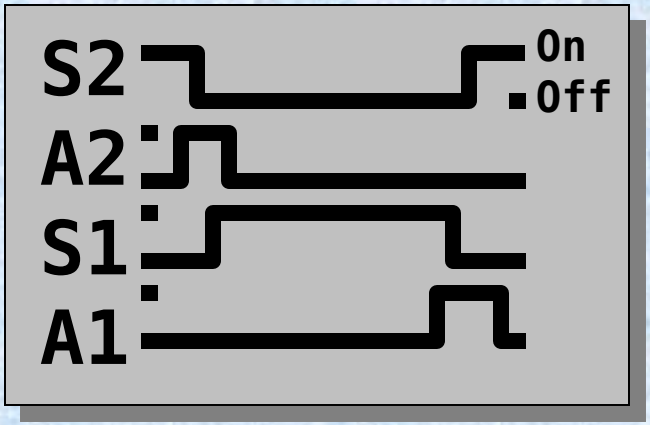
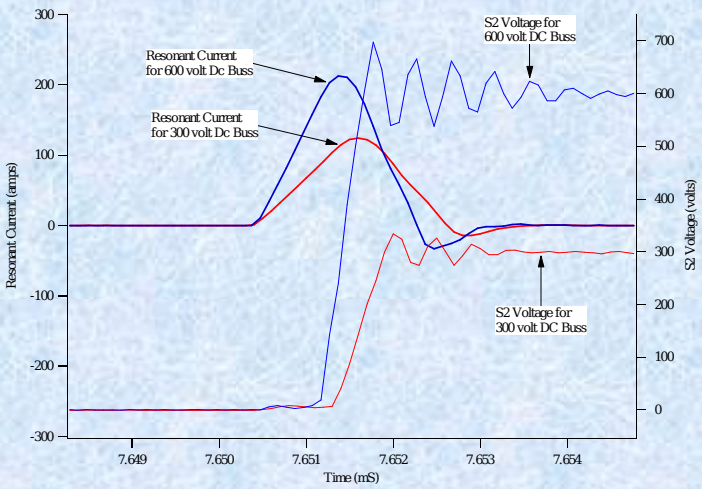


ARCP Operation

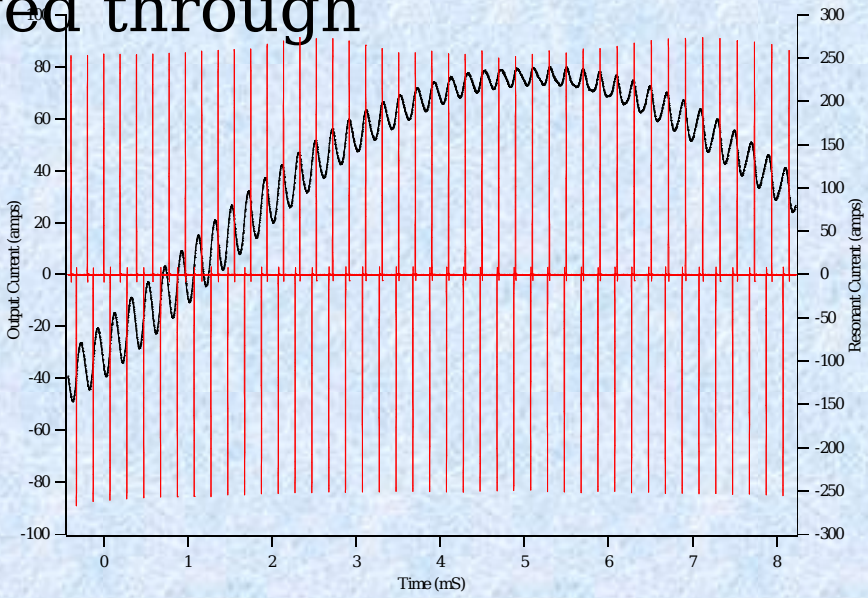
- Voltage across phase switch (S1 and S2) driven to 0 prior to their turn-on.
  - Accomplished by generating a resonant current pulse prior to S1 or S2 turn-on
  - Resonant pulse formed by turning on AC switch: di/dt = V/2*Lr
  - At proper moment, conducting phase switch is turned off
  - Resonant current follows trajectory governed by Lr*Cr resonant component values
    - (see Ref [1] - DeDoncker for ARCP details)





Resonant Pulse Control

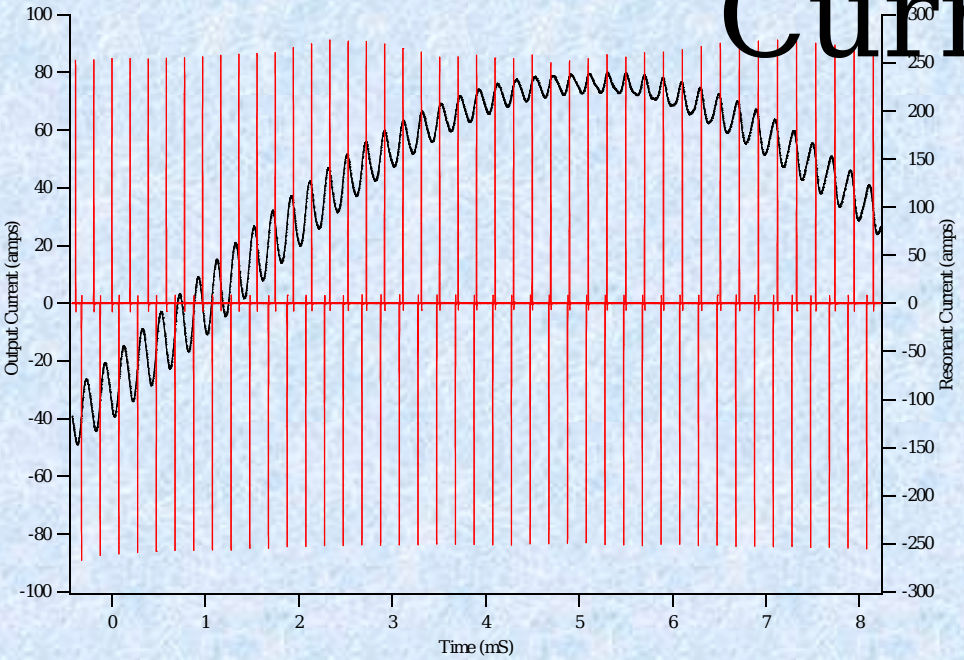
- Original testing done using fixed time between AC switch turn-on and conducting phase switch turn-off
  - Set for worst case load current
  - Meant that most of the time, excessive resonant current flowed through components

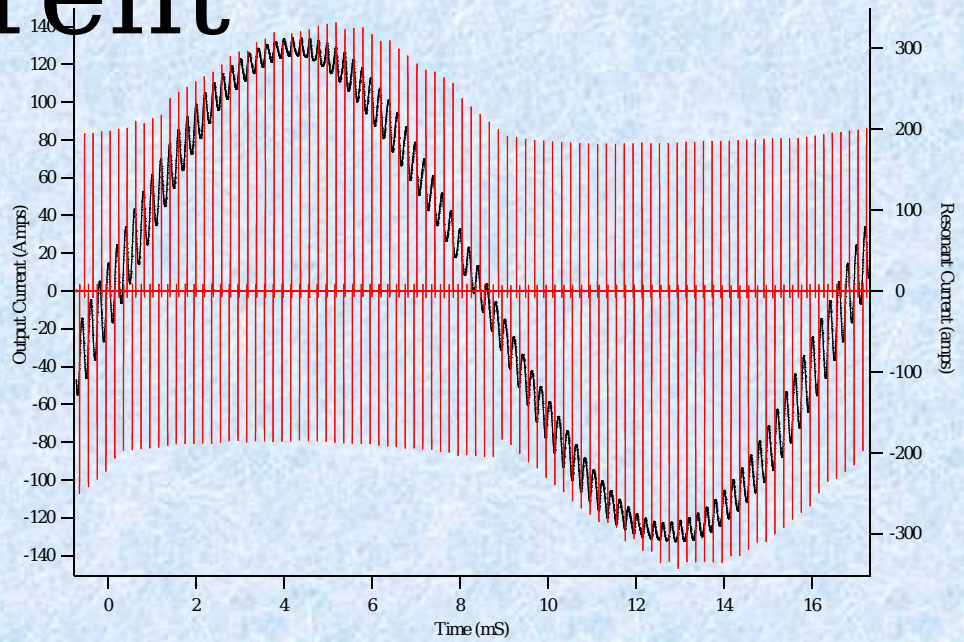


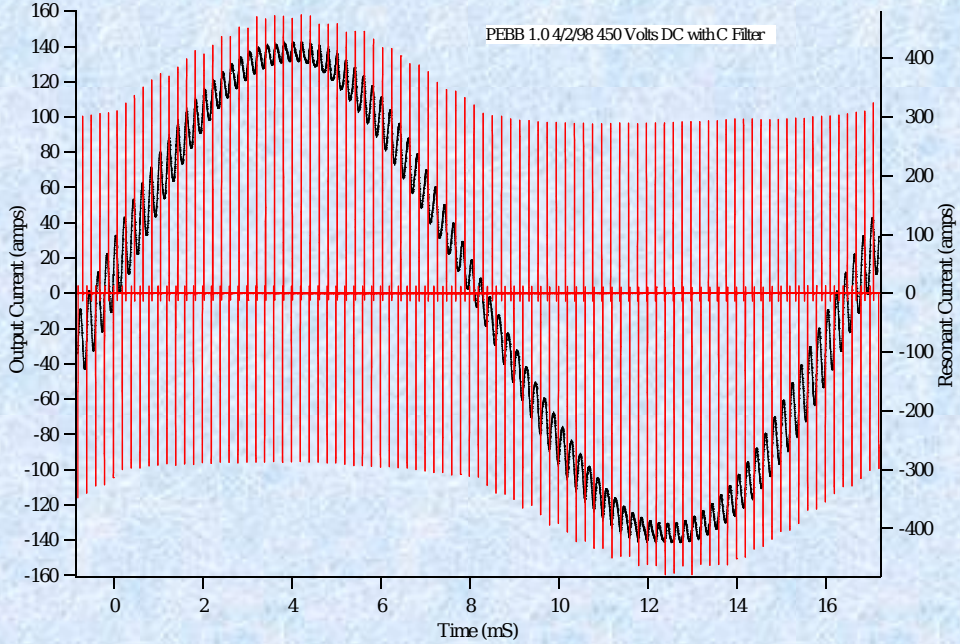
Resonant Pulse Control

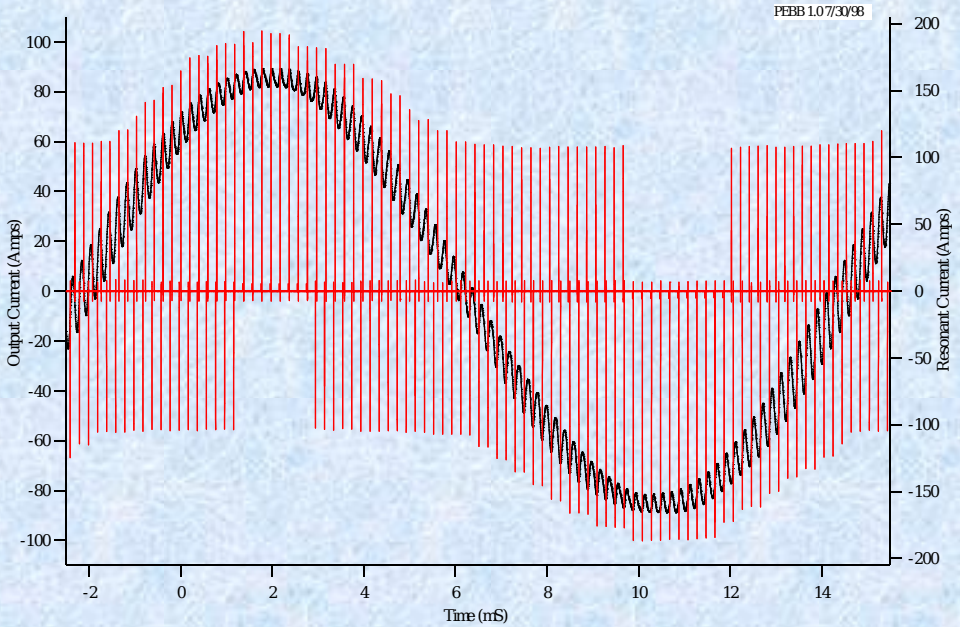
- Steps to improve resonant energy usage
  - Modulate resonant current based upon DC bus voltage and instantaneous load current magnitude and direction
    - Vdc - low bandwidth, 1% resolution
    - Ioutput - 3 samples within 120 degrees of switching frequency, 12 bit resolution
  - Resonant current pulse inhibit when load current is sufficient to achieve zero voltage transition

Steps to Minimize Resonant Current

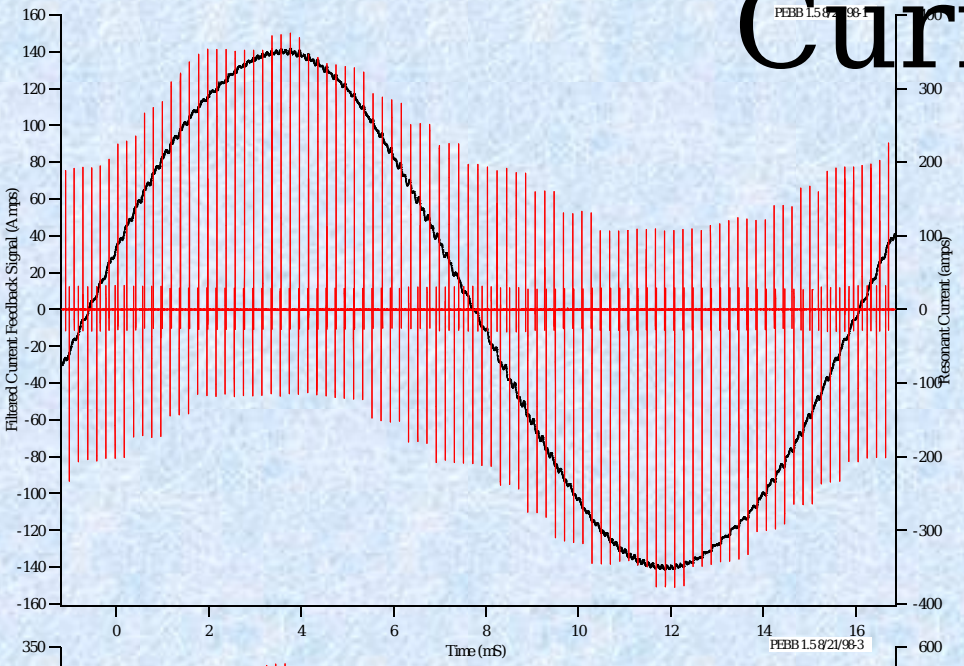


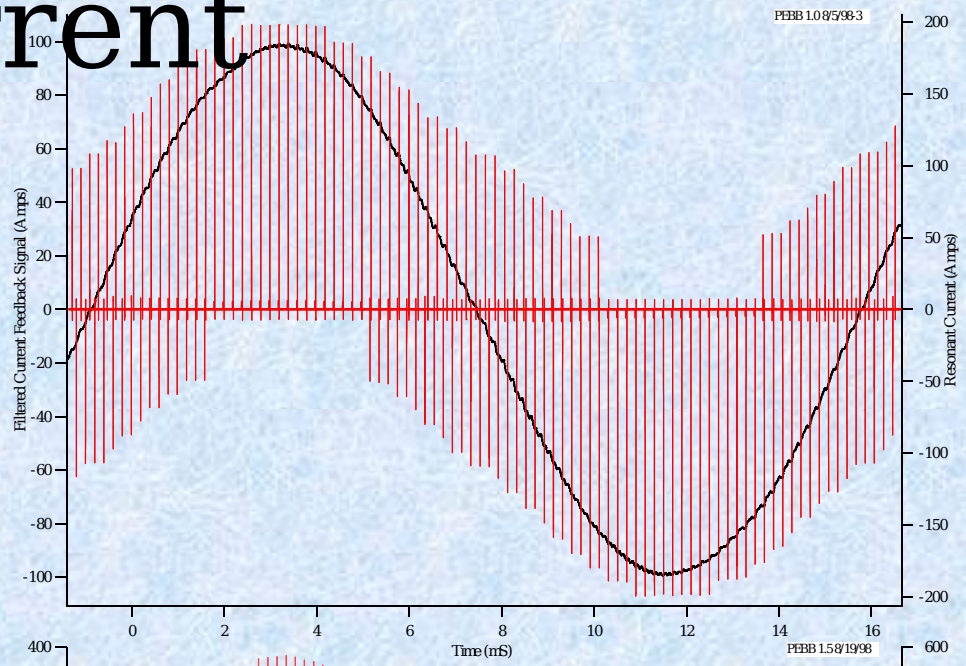


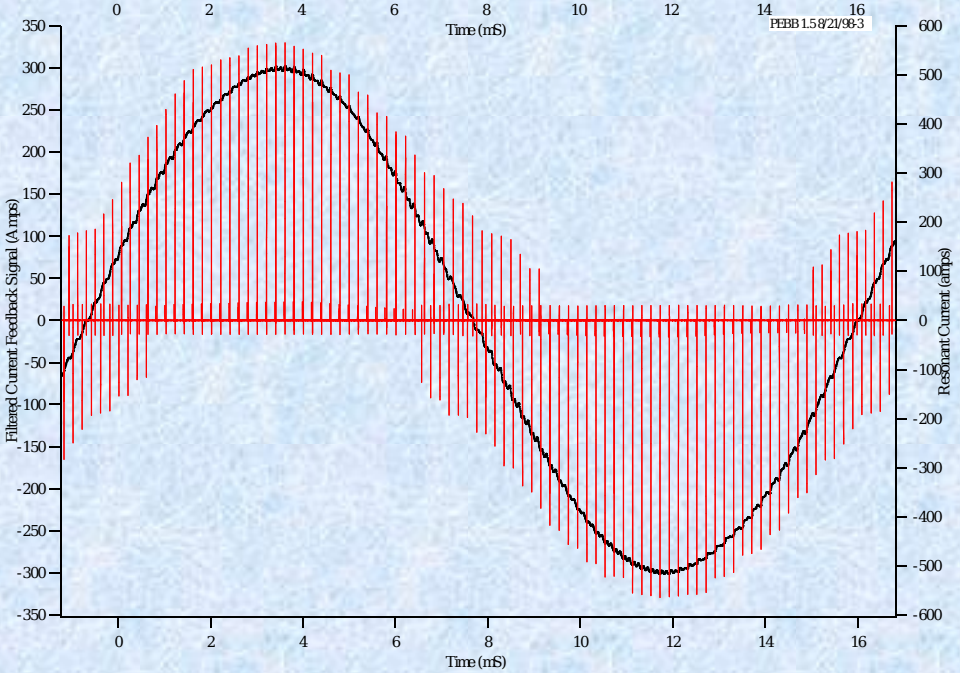


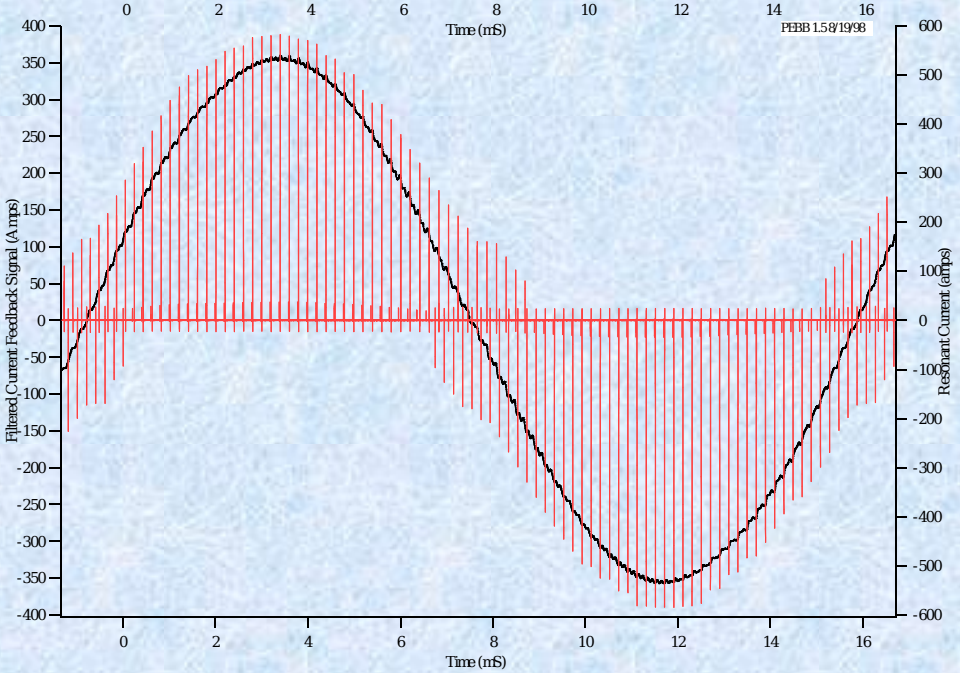


Steps to Minimize Resonant Current









Background

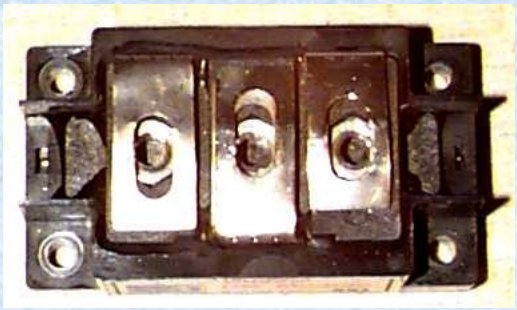
- Chosen topology - Auxiliary Resonant Commutated Pole (ARCP) zero voltage switching inverter
  - Navy had previously worked with GECR&D on ARCP as a candidate for DC-AC ship service inverter module (SSIM) application under the Navy's Integrated Power System (IPS) Program.
- NSWC used the GE design as its starting point using core elements produced by Harris

Background

- ARCPs that have been built at NSWC
  - PEBB1 - based
    - pMCTs as both main and auxiliary switches
    - IGBT main switches, pMCT auxiliary switches
  - PEBB1.5 - based
    - Non-punch-through IGBT main switches, combination of p and nMCT auxiliary switches

Background

- PEBB1 Core Devices
  - Half Bridge Module
    - pMCTs
    - npt IGBTs
  - AC Module
    - pMCT
  - Gate Drive
    - Includes Jumper for Zero Voltage Turn-on Logic for Half Bridge
  - Water Cooled Heatsink



HARRIS SEMICONDUCTOR

PRELIMINARY

150A, 1200V

January-98

AC Switch With P-Type MOS Controlled Thyristor (MCT)

Features

150A, 1200V
Low Conduction Loss
Four Quadrant switch
5kA Surge Current Capability
80kA/us di/dt Capability
Low Gate Drive Power
300A Gate Turn-Off Capability at +150°C
Isolated Base Plate for Easy Heat Sinking

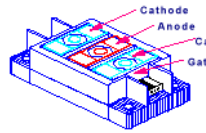
Description

The MCT is a MOS Controlled Thyristor designed for switching current on and off by negative and positive pulsed control on an insulated MOS gate. It is designed for use in motor controls, inverters, line switches and other power switching applications.

The MCT is especially suited for resonant (zero voltage or zero current switching) applications. The SCR like forward drop greatly reduces conduction power loss.

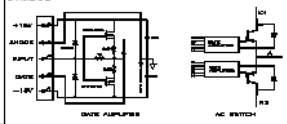
MCTs allow the control of high power circuits with very small amounts of input energy. They feature the high peak current capability common to SCR type thyristors, and operate at junction temperature up to +150°C with active switching.

PACKAGE SIZE 3.20" X 1.76"
2 SIZE-8 P-MCTS (1cm²) & 2 SIZE-7 DIODES (0.6cm²)



PEBB1 AC Switch Module

SYMBOL



Absolute Maximum Ratings At T_C=+25°C, Unless Otherwise Specified

	SYMBOL		UNITS
Peak Off State Voltage	V_{DRM}	+/-1200	V
Continuous Cathode Current (T_C = +90°C)	I_{K90}	150	A
Non-Repetitive Peak Cathode Current (Note 1)	I_{KSM}	5000	A
Peak Controllable Current	I_{KC}	300	A
Gate to Anode Voltage (Continuous)	V_{GA}	+/-15	V
Gate to Anode Voltage (Peak)	V_{GAM}	+/-20	V
Rate of Change of Voltage (V_{DA} = 15V)	dv/dt	10000	V/us
Rate of Change of Current	di/dt	80000	A/us
Maximum Power Dissipation	P_T	400	W
Operating and Storage Temperature	T_J, T_{STG}	-40 to +150	°C
Maximum Temperature for Soldering	T_L	250	°C

NOTE:
1. Maximum Pulse Width of 200us (Half Sine) assume T_J (Initial) = +90°C and T_J (Final) = T_J (Max) = +150°C

Electrical Specifications At T_C = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Peak Off-State	I_{DRM}	V_{KA} = -1200V	Tc = +150°C	-	-	2.5	mA
Blocking Current		V_{GA} = +9V	Tc = +25°C	-	-	200	uA
On State Voltage	V_{TM}	I_K=200A	Tc = +150°C	-	1.8	2.0	V
		V_{GA} = -9V	Tc = +25°C	-	1.8	2.0	V
Gate to Anode Leakage Current	I_{GAS}	V_{GA} = +/-15V		-	-	450	nA
Gate to Anode Capacitance		Per MCT		-	43	-	nF
Gate Amplifier Input Charge		+/-15V		-	-	150	nC
Thermal Impedance	$R_{\Theta JC}$	Per MCT		0.12	-	0.18	°C/W
Junction to Case		Per Diode		0.18	-	0.27	°C/W
Diode Forward Drop	V_F	I_K=200A	Tc = +150°C	-	2.3	2.5	V
			Tc = +25°C	-	2.1	2.3	V
Reverse Recovery Current		T_J = +125°C; V_{DA} = +/-15V		-	55	-	A
Voltage Over-Shoot		I_K = 500A; di/dt = 170A/uS		-	150	-	V
[illegible]gy Dissipation		$C_{snubber}$ = 33 nF; $R_{snubber}$ = 10 Ohm		-	8.5	-	mJ

E:
ecommended Gate Voltage Slew Rate (V_{GA}) from -12V to +15V is less than 200ns.

Caution: Preliminary Data. Data shown is subject to change.

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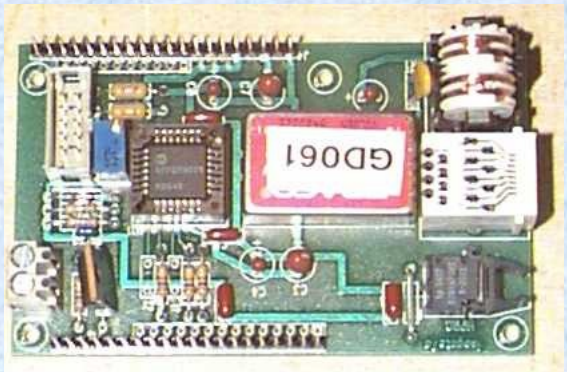
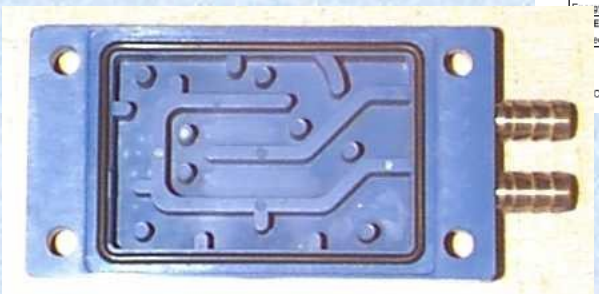
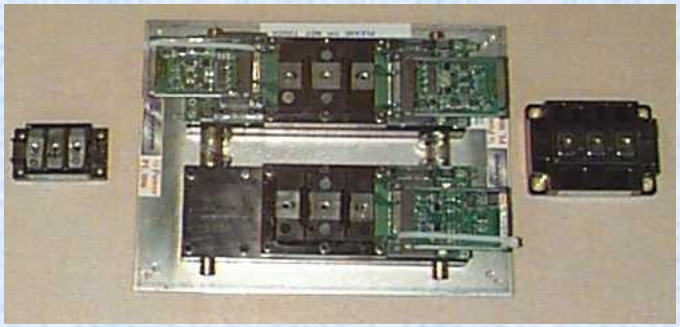
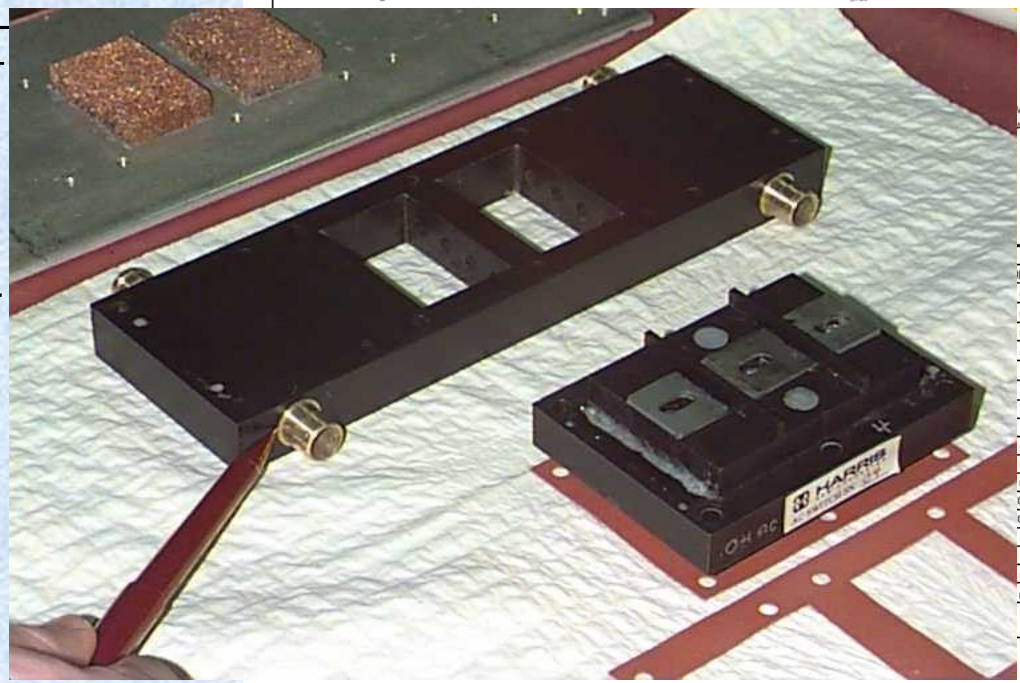




Background

- PEBB1.5 Core Devices
  - Half Bridge Module
    - npt IGBTs
  - AC Module
    - one pMCT one nMCT
    - snubber resistor
  - Gate Drives
  - Heat Sink Assembly





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Low Conduction Loss
Low Gate Drive Power
300A Gate Turn-Off Capability at +150°C
Isolated Base Plate with Copper Sponge for Easy Heat Sinking
Temperature Sensor

Description

The MCT is a MOS Controlled Thyristor designed for switching current on and off by negative and positive pulsed control on an insulated MOS gate. It is designed for use in motor controls, inverters, line switches and other power switching applications.

The MCT is especially suited for resonant (zero voltage or zero current switching) applications. The SCR like forward drop greatly reduces conduction power loss.

MCTs allow the control of high power circuits with very small amounts of input energy. They feature the high peak current capability common to SCR type thyristors, and operate at junction temperature up to +150°C with active switching.

PACKAGE SIZE 4" X 3" x 1.25"

1 P-MCT & 1 N-MCT S-8 (1cm²) & 2 S-7 DIODES (0.6cm²)

R D S Control

PEBB1.5 AC Switch Module

SYMBOL

AC SWITCH

Absolute Maximum Ratings At T_C=+25°C, Unless Otherwise Specified

	SYMBOL		UNITS
Peak Off State Voltage	V_{DRM}	+/-1200	V

Caution: Preliminary Data. Data shown is subject to change.

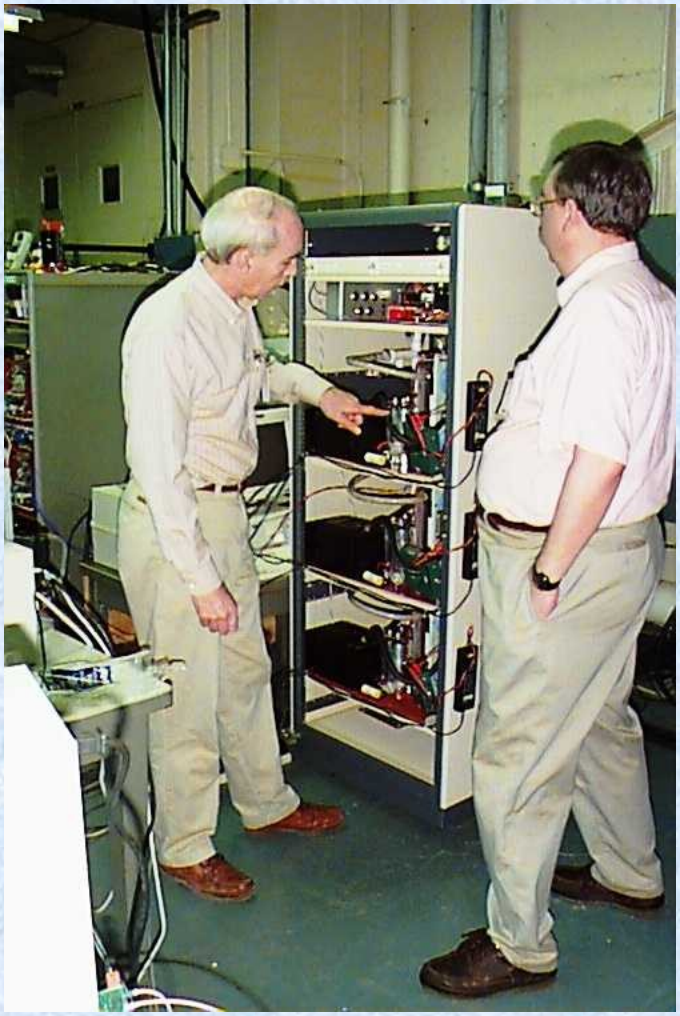
Copyright Harris Corporation 1998

PEBB 1 Hardware

- Qty of 4 three phase units
  - Main switch - PMCT
  - Aux Switch - PMCT
  - DC Bus Caps - orig. 7000uF
    - reduced to 3500uF per phase
  - Resonant inductor - 1.6uH
  - Resonant Cap - .8uf per switch
    - 1.6uf total per phase
  - Resonant frequency ~ 100kHz
  - Output filter - 175uH, 50uF
  - Controller TMS320 DSP
    - 100ns step control of ac switch on time
    - at 800vdc = 40 amp step control

PEBB 1.5 ARCP Inverter

- Design Specifications: DC-AC operating mode
  - Input: 750 - 850Vdc
  - Output: 450Vac RMS at 250kW (water cooled)
- Major Components
  - Main switch - NonPunchThrough IGBT
  - Aux. Switch - Combo N-and P-MCT
  - DC Bus Caps - 6900 uF per phase
  - Resonant inductor - 1.0-1.2 uH
  - Resonant Cap - .1 uF/switch, .2uF/phase
  - DSP Based Digital Controller
    - 100ns step control of ac switch on time
    - at 800vdc = 40 amp step control
- Present status
  - Assembly completed 4/3/98
  - Tested up to 200kW 10/98



Perceived Benefits of ARCP

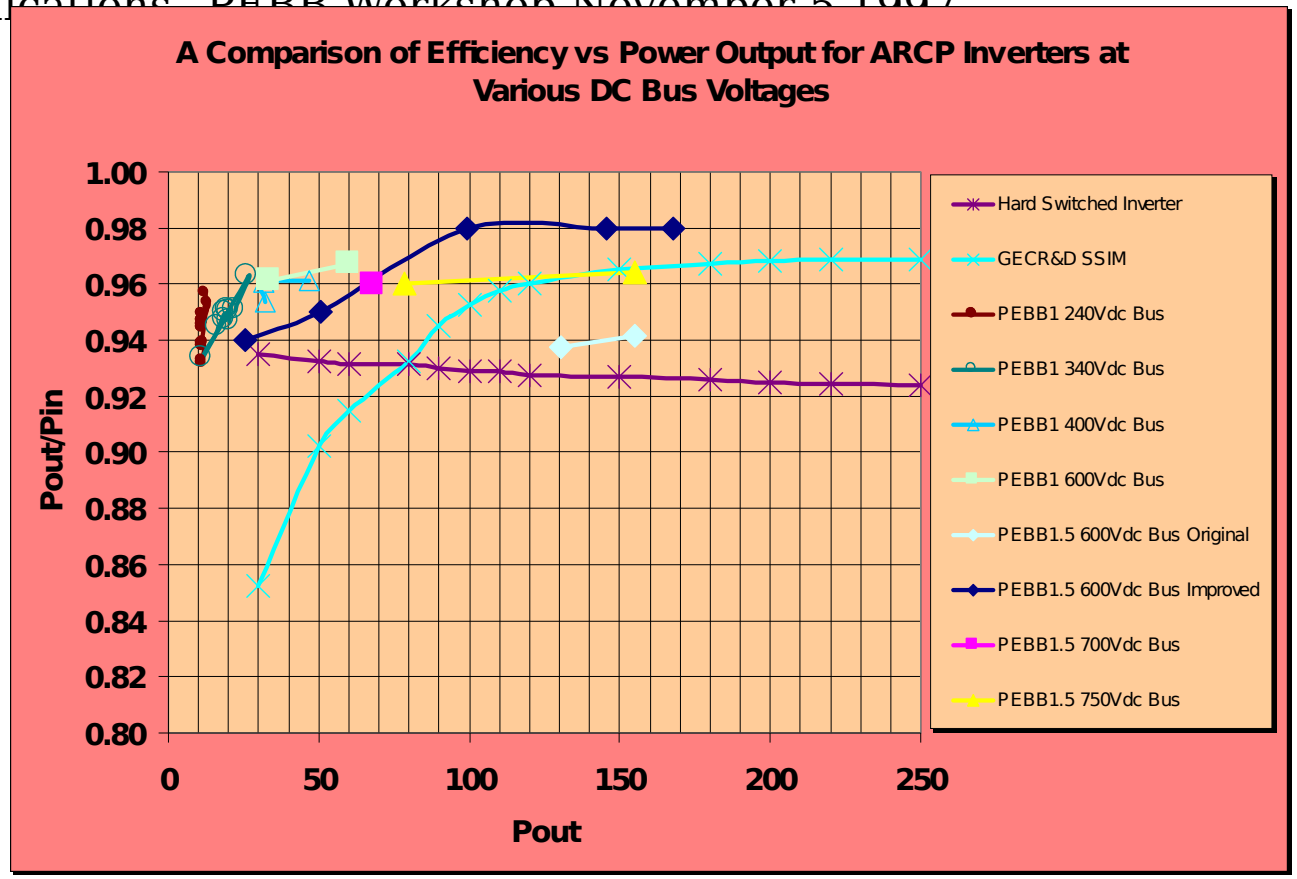
- Lower Loss/Higher Efficiency
- Lower Device Stress, Lower High Frequency EMI, Friendlier to the load in terms of dV/dt and dI/dt

Perceived Benefits of ARCP

- Lower Loss/Higher Efficiency
  - An ARCP inverter was designed built and tested by PSU under NSWC PEBB contract to investigate high frequency converter issues
    - IGBT Main switches/FET auxiliary
    - ARCP operation 190V, 14A output - 63.4 kHz switching frequency
    - Disabled auxiliary circuit and operated as hard switched inverter at same output voltage and current
      - Switching frequency slowly increased until failure occurring at 32.5kHz
    - [1] Salberta, Frederick; Mayer, Jeffrey S.; and Cooley, Roger T., “An improved Control Strategy for a 50kHz Auxiliary Resonant Commutated Pole Converter,”Power Electronics Specialist Conference St Louis MO June 22-27th 1997

Perceived Benefits of ARCP

- Lower Loss/Higher Efficiency
- [2] Keraluwala, Mustansir; Szczesny Paul; Esser, Albert and Hegner, Henry, “Development of a 250kVA, High Performance, Ship Service Inverter Module (SSIM) for Future Naval Applications,” Power Electronics Applications, PEBB Workshop November 5 1997



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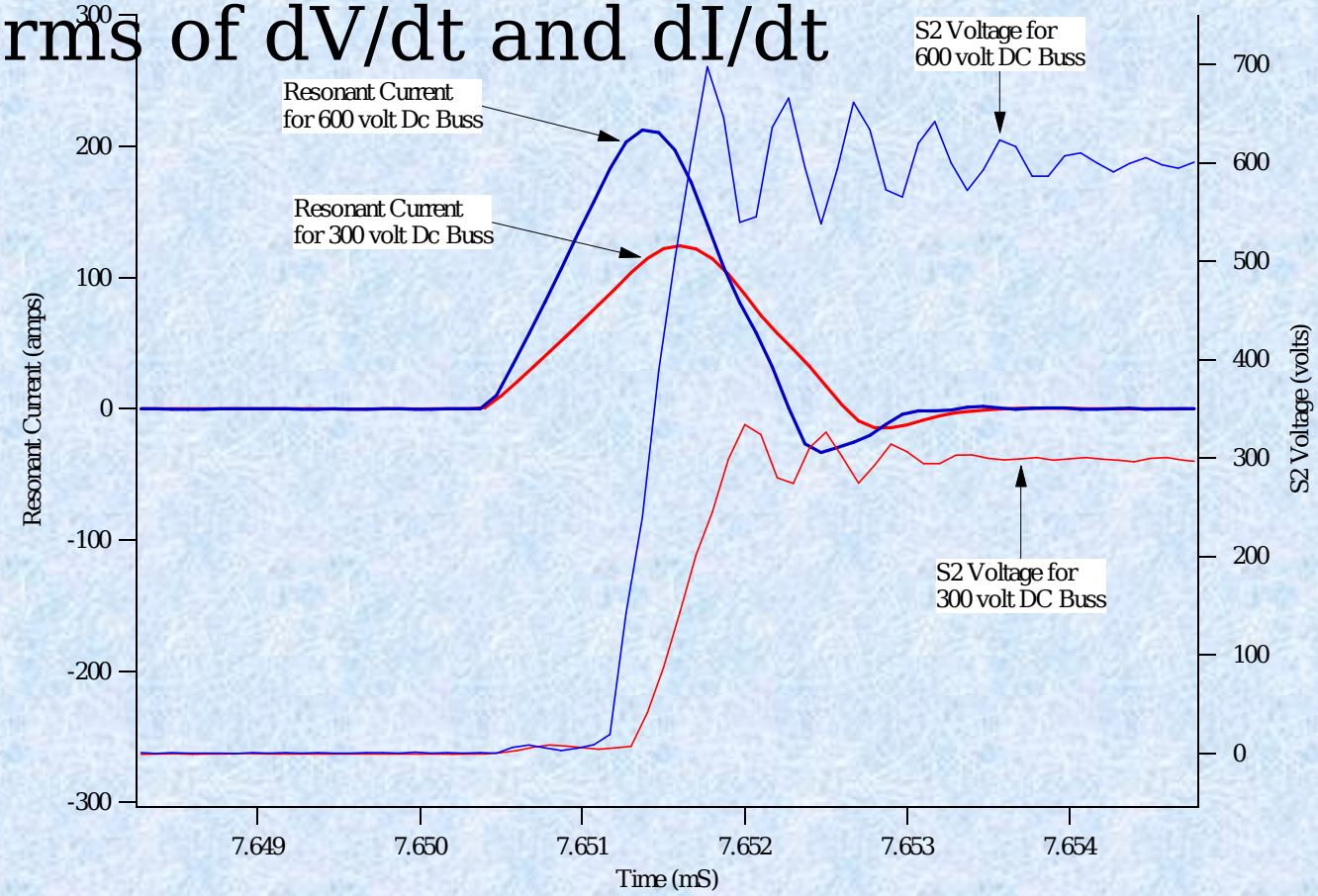
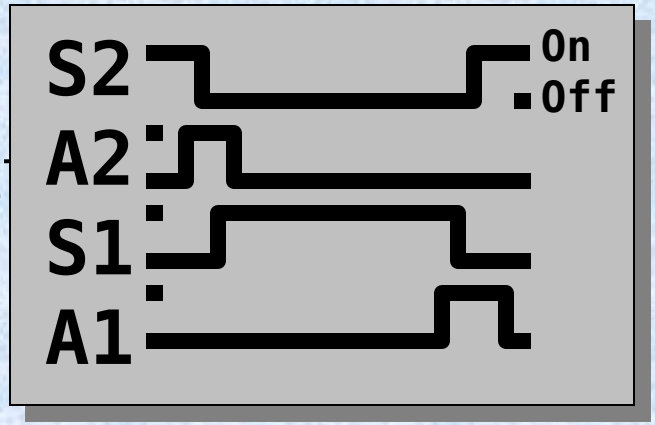
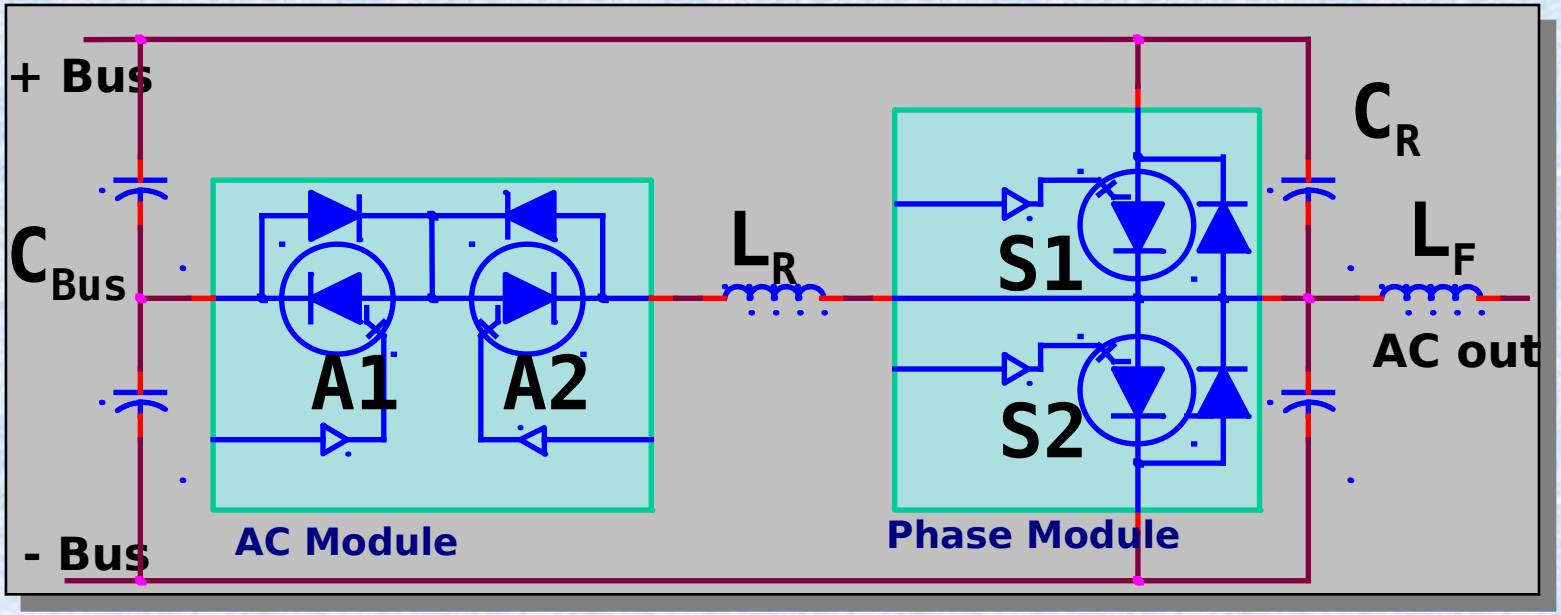


Perceived Tradeoffs

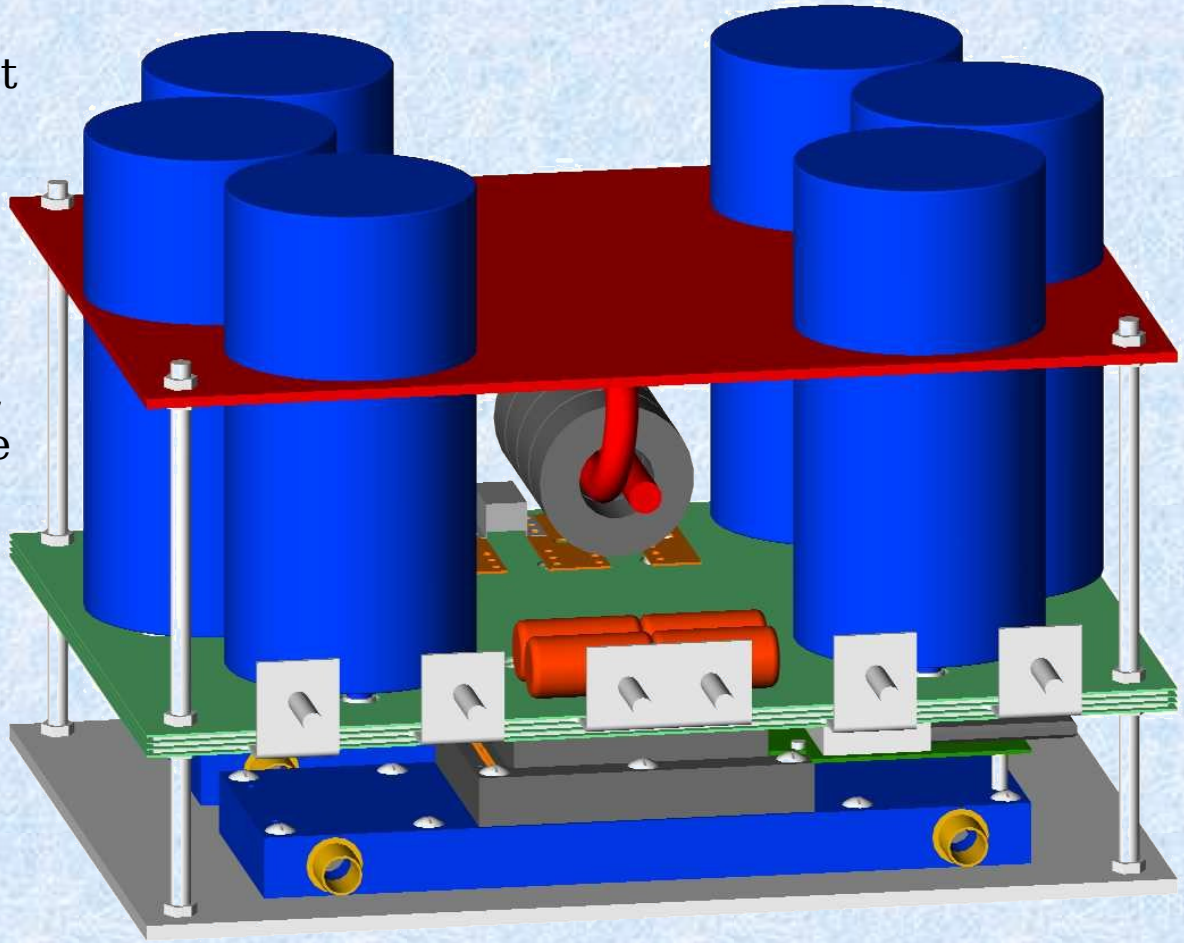
- Higher parts count
- Controller Complexi
- Higher cost





Perceived Tradeoffs

- Higher parts count
  - DC bus cap function
    - supply resonant current pulses (soft switching only)
    - supply HF ripple demanded by PWM (hard switch demand may be worse than soft switch due to the shape of the demanded voltage waveform -square wave vs trapezoid)
    - could end up being a wash



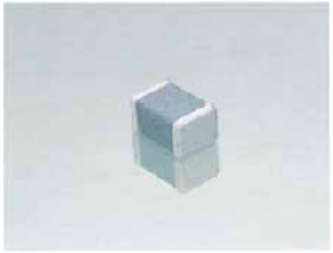
Perceived Tradeoffs

- Parts Count - Resonant Inductor
  - L value relatively low ~ 1.0 - 1.5uH
    - High frequency current components
      - Litz wire used
    - L value subject to variability in manufacture
    - L value subject to variability under operation due to temperature fluctuations (this has not yet been measured)
  - Not having a stable value inductor limits how close controller can push safety margins

Perceived Tradeoffs

- Parts Count - Resonant Capacitor
  - Requires accurate known value with little or no temperature drift
  - Quantity needed dependent on tail current of Phase switch
  - Expensive

NPO Dielectric
General Specifications



NPO is the most popular formulation of the "temperature-compensating," EIA Class I ceramic materials. Modern NPO formulations contain neodymium, samarium and other rare earth oxides.

NPO ceramics offer one of the most stable capacitor dielectrics available. Capacitance change with temperature is 0 ±30ppm/°C which is less than ±0.3% Δ C from -55°C to +125°C. Capacitance drift or hysteresis for NPO ceramics is negligible at less than ±0.05% versus up to ±2% for films. Typical capacitance change with life is less than ±0.1% for NPOs, one-fifth that shown by most other dielectrics. NPO formulations show no aging characteristics.

The NPO formulation usually has a "Q" in excess of 1000 and shows little capacitance or "Q" changes with frequency. Their dielectric absorption is typically less than 0.6% which is similar to mica and most films.

Part Number (see page 3 for complete information and options)

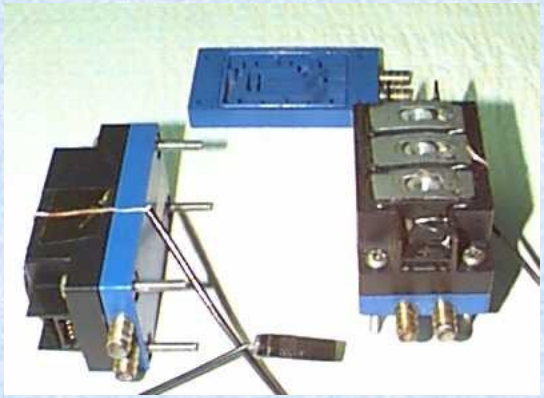
0805	5	A	101	K	A	T	2	A
Size (L" x W")	**Voltage** 50V = 5 100V = 1 200V = 2	**Dielectric** NPO = A	**Capacitance Code**	**Capacitance Tolerance** Preferred K = ±10% J = ± 5%	**Failure Rate**	**Terminations** T = Plated Ni and Solder	**Marking Packaging** 2 = 7" Reel Paper/Unmarked	**Special Code** A = Std. Product

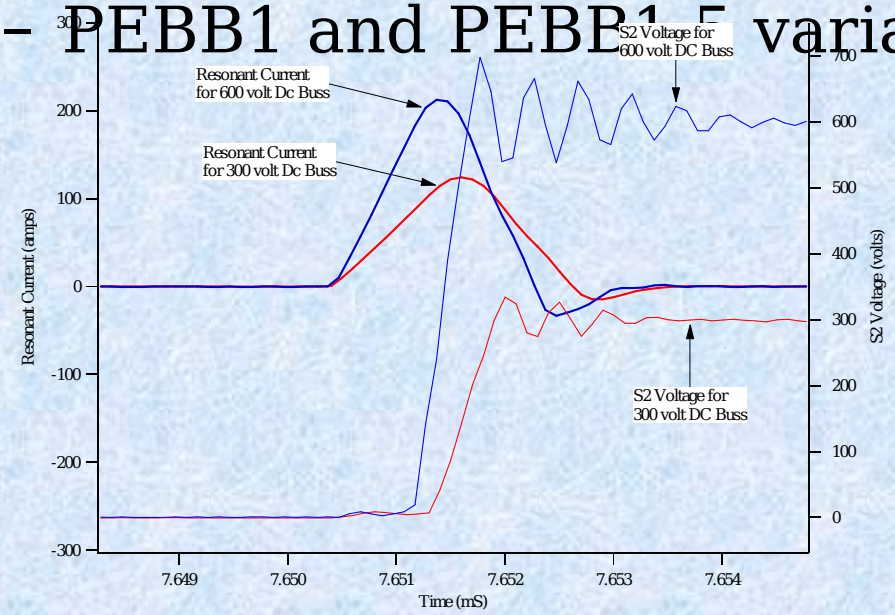
Performance Characteristics: NPO

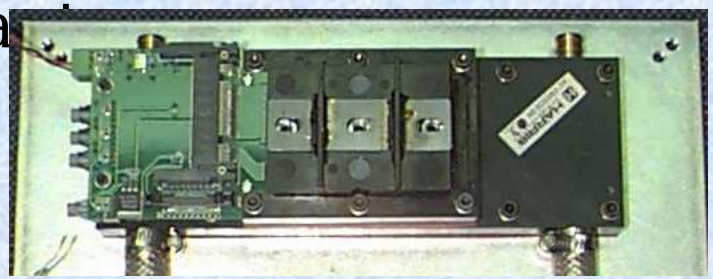
Capacitance Range	0.5 pF to .033 µF (1.0 ±0.2 Vrms, 1kHz, for ≤100 pF use 1 MHz)
Capacitance Tolerances	Preferred ±5%, ±10% others available: ±.25 pF, ±.5 pF, ±1% (≥25pF), ±2%(≥13pF), ±20% For values ≤ 10 pF preferred tolerance is ±.5 pF, also available ±.25 pF.
Operating Temperature Range	-55°C to +125°C
Temperature Characteristic	0 ± 30 ppm/°C
Voltage Ratings	25, 50, 100 & 200 VDC (+125°C)
Dissipation Factor and "Q"	For values >30 pF: 0.1% max. (+25°C and +125°C) For values ≤30 pF: "Q" = 400 + 20XC (C in pF)
Insulation Resistance (+25°C, RVDC)	100,000 megohms min. or 1000 MΩ - µF min., whichever is less
Insulation Resistance (+125°C, RVDC)	10,000 megohms min. or 100 MΩ - µF min., whichever is less
Dielectric Strength	250% of rated voltage for 5 seconds at 50 mamp max. current
Test Voltage	1 ± 0.2 Vrms
Test Frequency	For values ≤100 pF: 1 MHz For values >100 pF: 1 KHz

Perceived Tradeoffs

- Parts Count - Auxiliary switch
  - needs to supply very high di/dt pulse
  - zero current turn off
  - PEBB1 and PEBB1.5 variant



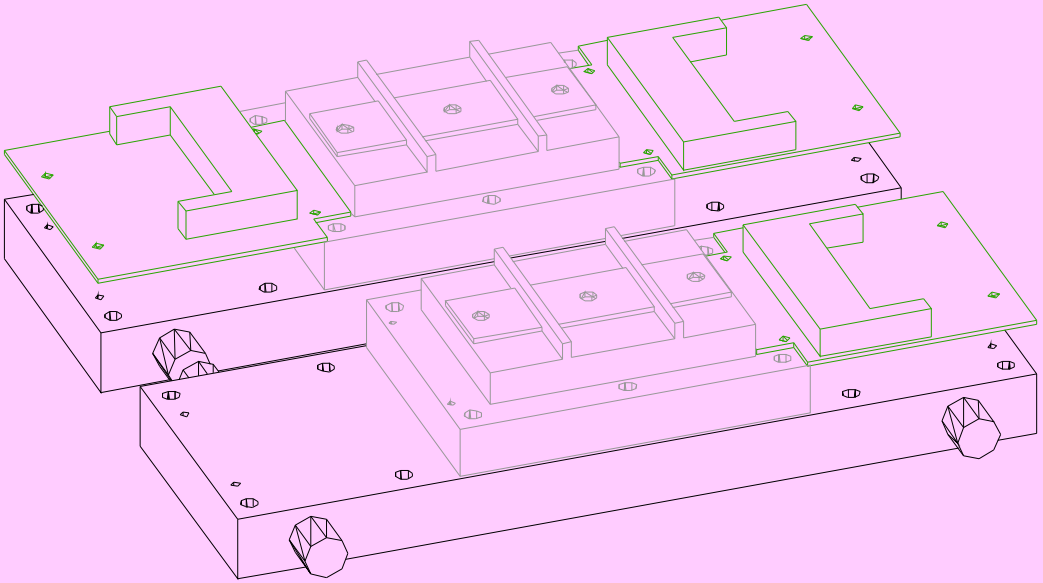




Perceived Tradeoffs

- Parts Count - feedback signals needed
  - Soft Switch Transition
    - Vdc - low bandwidth, 1% resolution
    - Ioutput - 3 samples within 120 degrees of switching frequency, 12 bit resolution
  - Voltage Regulation
    - Vout - update at switching frequency, 1% resolution

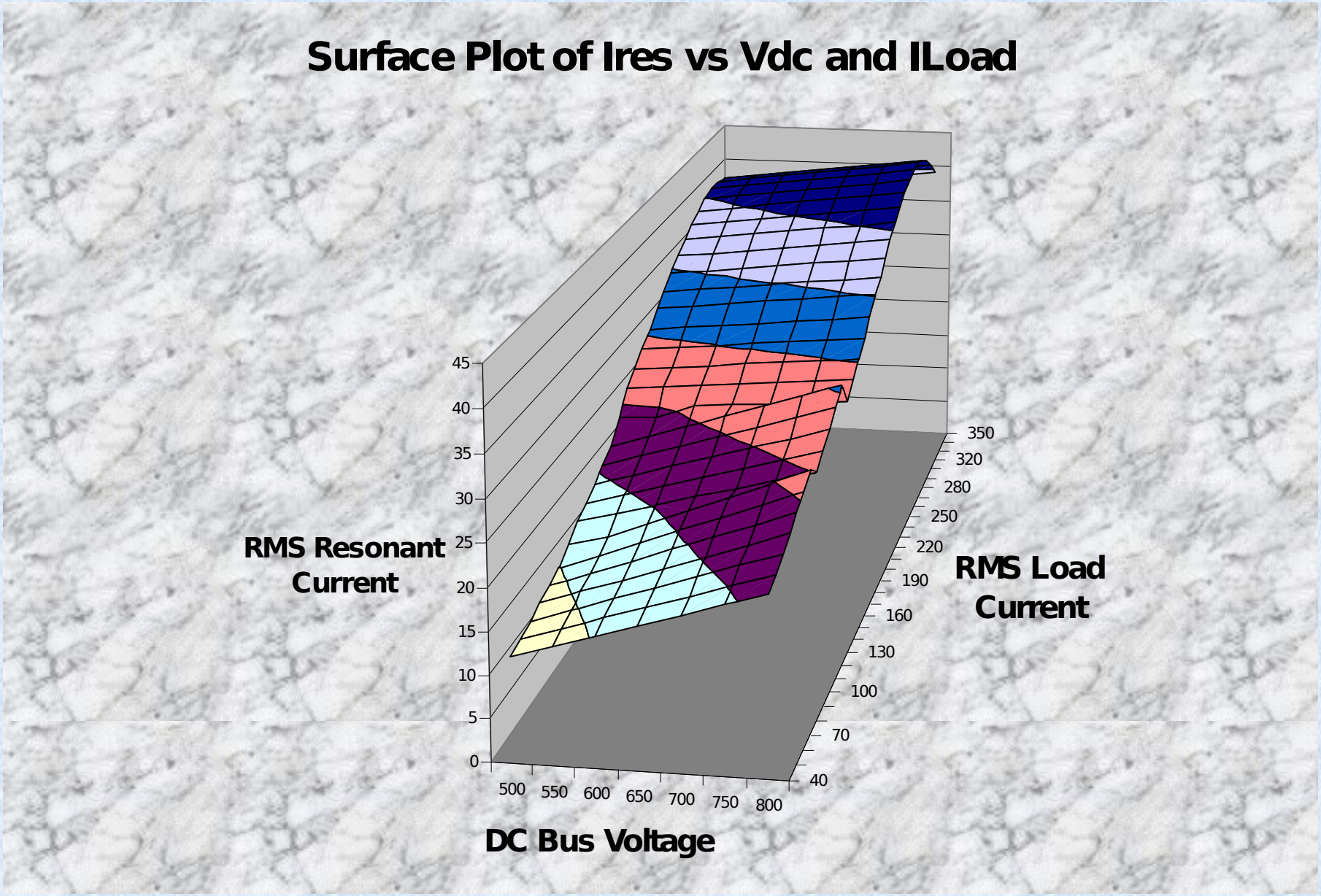
Perceived Tradeoffs



- Higher cost
  - The goal of the PEBB program is to develop an automated manufacturing process using pick and place assembly techniques to produce a module employing the proper types of semiconductor switches, diodes and ultimately passive and control components interconnected in the circuit topology requested by the circuit designer
  - Harris PEBB1.5 modules employing HTP semiconductor die in a generic, user definable arrangement begin to demonstrate a way of removing the costly hand assembly process from power converter manufacturing

Perceived Tradeoffs

- A significant amount of effort was made in order to minimize the cost and size impact of the additional components required for ARCP
- The key was to supply the minimum amount of resonant energy to allow a zero voltage transition to occur
- This would minimize the current handling requirements of the additional components



Projects to approximately 50A rms resonant current for

Issues uncovered during analysis and testing

- Output filter design and manufacturing
  - hard to find inexpensive, compact, high fre

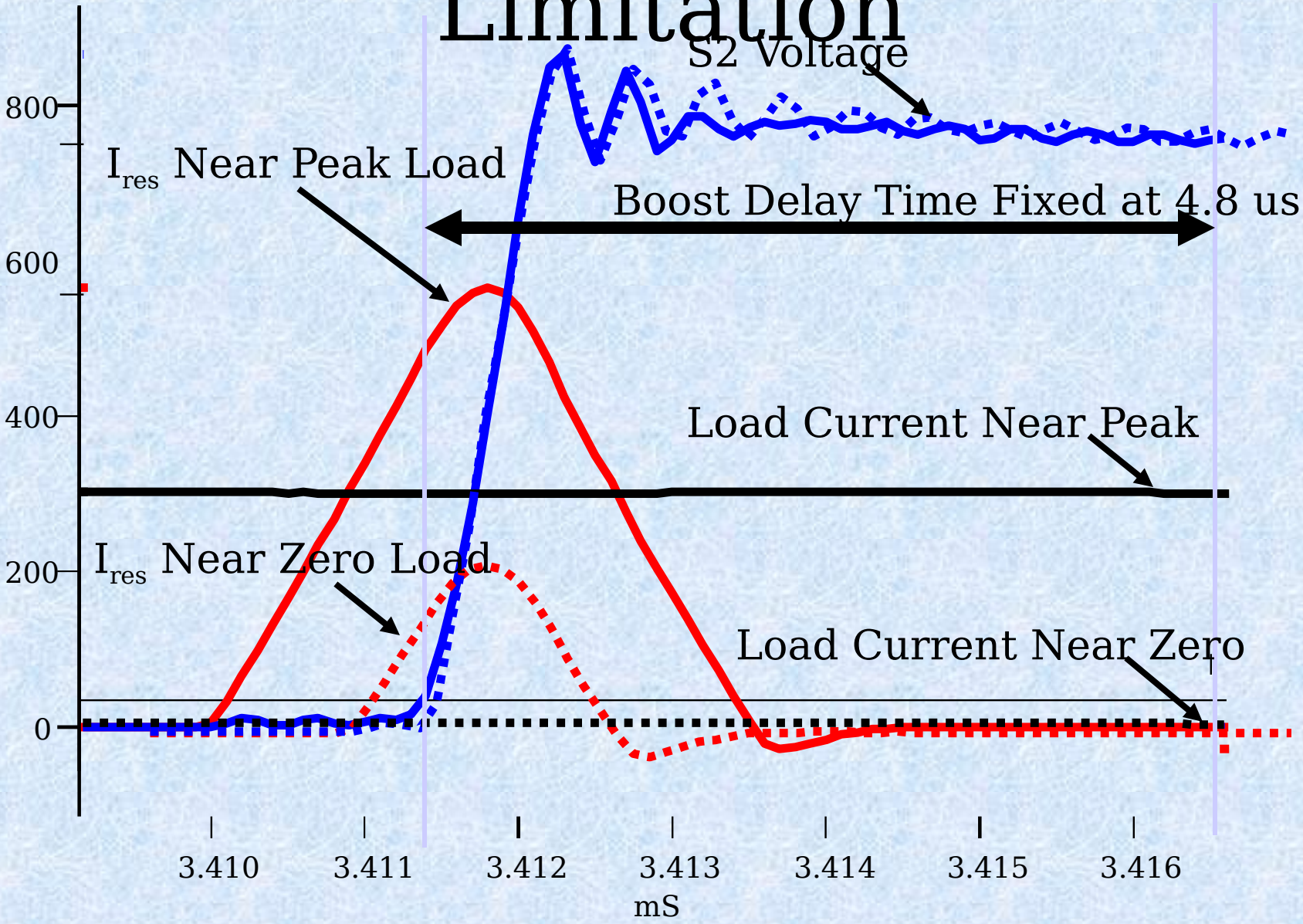
Issues uncovered during analysis and testing

- Present Controller Implementation has data sampling latency times which compromise performance
- Loss of duty cycle due to resonant pulse times and above latency times
- Difficult to design into controller enough safety margins to operate within real world limitations of chosen devices, yet have enough performance to compete with a hard switched converter

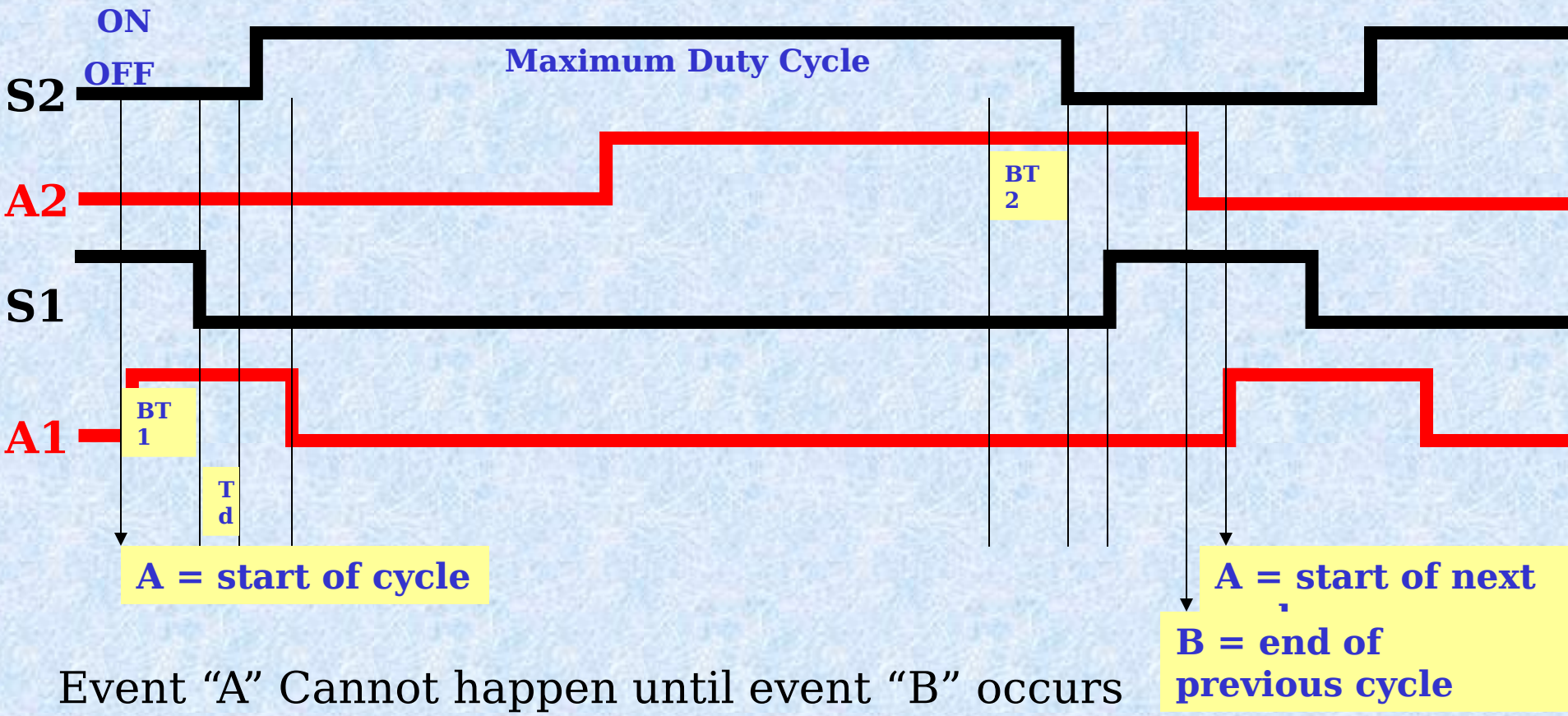
Issues uncovered during analysis and testing

- Dropping out of ARCP (zero voltage transition) mode due to insufficient boost or failure of a phase switch to latch to the output node of the appropriate rail results in AC switch supplying load current
- In the present implementation, the AC switch eventually tries to turn off this current
- Small snubber circuit in place is insufficient to allow AC switch to survive this occurrence

Maximum Duty Cycle Limitation



Maximum Duty Cycle Limitation



Event “A” Cannot happen until event “B” occurs
Event “B” cannot complete until resonant current pulse = 0
That time is not readily known, so a worst case Boost delay time of

Maximum Duty Cycle Limitation

$$V_{LL} = 0.612 * V_{dc} [2d_{max} - 1]$$

- It is estimated that next generation controller will enable reducing latencies and dead times by up to 5us.
- A 10% improvement in duty cycle utilization corresponds to a 20% improvement in available Line to Line Voltage
- Note: Third Harmonic Injection will increase V_{LL} by 15%

Conclusion

- The NSWC PEBB as presently implemented as an ARCP inverter has been demonstrated at 200kW.
- On-going refinements are continuing, which allow the ARCP to achieve higher performance and multiple power conversion functions.

Conclusion

- The areas where improvements can be made to narrow the gap are:
  - A method of partitioning ARCP-specific control circuitry as close to the phaseleg as possible in order to allow traditional controllers to be employed
  - An automated module assembly process that would allow the ARCP to be easily manufactured with minimal hand assembly
  - less expensive high performance capacitors and inductors

Voltage Balance

- Initial ARCP tests revealed several volts of unbalance between the three phases
- Control software was modified to compensate for two contributing factors
  - Differing resonant inductor charge times within the switching cycle were accounted for
  - Compensation for 1/3rd of switching cycle between phases
- Improved voltage unbalance from 1.47% to 0.1%